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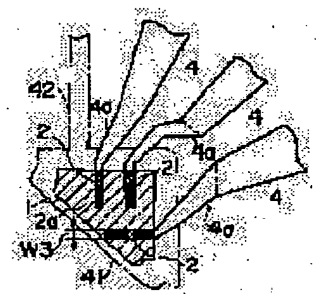
(54) ELECTRONIC DEVICE MANUFACTURED BY ANODE COUPLING AND MANUFACTURE THEREOF

(57)Abstract:
PURPOSE: To obtain a semiconductor device, and a manufacturing method thereof, in which the inner leads can be bonded collectively to a plurality of electrodes with high electrical and mechanical bonding strength.
CONSTITUTION: A semiconductor chip 1 is applied, on the surface thereof, with an insulating coating 2a which is rendered conductive upon heating. An inner lead 4a is extended from a lead frame 4 while covering the top face of an electrode 2 and then the inner lead is subjected, at the forward end thereof, to anode coupling with the insulating coating 2a. Consequently, the inner lead 4 a is brought into pressure contact with the electrode 2 and coupled electrically therewith.



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CLAIMS

[Claim(s)]

[Claim 1] It has a circuit element with the electrode electrically connected with the conductor for current I/O. If it heats around said electrode, after adhering the insulating coat which becomes conductivity Electronic parts manufactured using the anode plate conjugation method which said conductor is contacted to said electrode, carries out anode plate junction of the insulating coat and said conductor of a superposition lever on said insulating coat, and is characterized by connecting said conductor and said electrode electrically.

[Claim 2] Avoid the electrode in which the insulating coat which will become conductivity if it heats on the surface of a semiconductor chip was prepared on said semiconductor chip front face, and it adheres. Where it has arranged the tip of the inner lead installed from the leadframe on said insulating coat so that this electrode may be covered, and these are piled up, while carrying out anode plate junction of the tip of this insulating coat and said inner lead Electronic parts manufactured using the anode plate conjugation method characterized by connecting this inner lead and electrode electrically.

[Claim 3] Electronic parts manufactured using the anode plate conjugation method according to claim 2 characterized by adhering a metal coat on the insulating passivation film prepared on the surface of the semiconductor chip.

[Claim 4] Electronic parts manufactured using the anode plate conjugation method according to claim 2 characterized by constituting the front face of the electrode on a semiconductor chip so that it may become higher than the maximum top face of the insulating coat to which the front face of said semiconductor chip adhered, and which will become conductivity if it heats.

[Claim 5] Electronic parts manufactured using the anode plate conjugation method according to claim 4 characterized by making the tip configuration of an electrode into a convex configuration.

[Claim 6] Electronic parts manufactured using the anode plate conjugation method according to claim 2 characterized by constituting the front face of the electrode on a semiconductor chip so that it may become lower than the maximum top face of the insulating coat to which the front face of said semiconductor chip adhered, and which will become conductivity if it heats.

[Claim 7] Electronic parts manufactured from the front face of said insulating coat using the anode plate conjugation method according to claim 5 characterized by laying the conductive matter with a small elastic modulus with which a part projects to the electrode prepared in the field lower than the front face of the insulating coat which becomes conductivity when heated.

[Claim 8] Electronic parts manufactured using the anode plate conjugation method according to claim 7 characterized by using mercury for the conductive matter.

[Claim 9] the insulating coat which will become conductivity if it heats on a part of front face of the inner lead by which anode plate junction was carried out on the semiconductor chip — adhering — wiring of the circuit board — a conductor — laying — said insulating coat and wiring — the electronic parts manufactured using the anode plate conjugation method according to claim 2 characterized by carrying out anode plate junction of the conductor.

[Claim 10] Electronic parts manufactured using the anode plate conjugation method according to claim 2 characterized by having made the end of the inner lead by which anode plate junction was carried out

refracted along with the edge of said semiconductor chip on a semiconductor chip, and casting to an out lead.

[Claim 11] If it heats on the surface of a semiconductor chip, while avoiding the electrode in which the insulating coat which becomes conductivity was prepared on said semiconductor chip front face and adhering Said semiconductor chip is mounted in the circuit board which carried out pattern NINGU of the piece. wiring electrically joined to said electrode — a conductor — the conductor which contacts except with said insulating coat — said insulating coat and conductor — carrying out anode plate junction of the piece — said electrode and wiring — the electronic parts manufactured using the anode plate conjugation method characterized by connecting a conductor electrically.

[Claim 12] The insulating coat which will become conductivity if it heats to a piece is adhered. wiring by which patterning was carried out to the 1st circuit board — the conductor by which was insulated from the conductor and patterning was carried out — Anode plate junction of the piece is carried out. said wiring — wiring which takes electrical installation to a conductor — a conductor and this wiring — the conductor insulated from the conductor — the 2nd circuit board to which patterning of the piece was carried out — said 1st circuit board — a laminating — carrying out — said insulating coat and conductor — Electronic parts manufactured using the anode plate conjugation method characterized by forming the laminating circuit board.

[Claim 13] wiring of an out lead of a semiconductor device — a conductor — the insulating coat which will become conductivity if it heats in a part of contact section — adhering — wiring of the circuit board — a conductor — a top — arranging — this insulating coat and wiring — the electronic parts manufactured using the anode plate conjugation method characterized by making a semiconductor device mount in the circuit board by carrying out anode plate junction of the conductor.

[Claim 14] The insulating coat which will become conductivity if it heats around this height while preparing a height at the tip of an inner lead is adhered. The crevice which adheres a metallic film to the perimeter of the electrode on a semiconductor chip by predetermined thickness, and reaches said electrode is formed. Electronic parts manufactured using the anode plate conjugation method characterized by having made said height engage with this crevice, having contacted said inner lead and said electrode, and carrying out anode plate junction of said insulating coat and said metallic film.

[Claim 15] The electronic parts which manufactured using the anode plate conjugation method characterized by to carry out anode plate junction of said insulating coat and said metallic film where prepared opening which reaches an inner lead in the insulating coat which becomes conductivity, and formed the crevice when it adhered at the tip of an inner lead and having been heated, and it made the convex electrode projected and prepared in this crevice from the metallic film on said front face of a semiconductor chip engaged and said inner lead and said electrode are contacted.

[Claim 16] Electronic parts manufactured using the anode plate conjugation method characterized by having carried out anode plate junction of said insulating coat and die pad, and fixing said leadframe pad to said semiconductor chip after adhering and laying the insulating coat which becomes conductivity in the die pad of a leadframe, when heated at the rear face of a semiconductor chip.

[Claim 17] The manufacture approach of the electronic parts which carry out alignment of the part for the point of each inner lead to the top face of an electrode after adhering the insulating coat which becomes conductivity to the front face of a semiconductor chip, if it heats on all the front faces except an electrode, and are characterized by connecting said each electrode and inner lead to coincidence electrically in the process which joins said each inner lead and said insulating coat with an anode plate conjugation method.

[Claim 18] On the front face of each semiconductor chip which carried out division separation and formed the semi-conductor wafer in plurality If it heats by all the front faces except an electrode adhering, in case the insulating coat and inner lead which become conductivity will be joined with an anode plate conjugation method After fitting into the crevice established in said insulating coat layer and inserting the conductive matter with a small elastic modulus in an electrode, The manufacture approach

of the electronic parts characterized by connecting said inner lead and said electrode electrically, carrying out the pressure welding of said conductive matter to said electrode in the process which carries out anode plate junction of said insulating coat and said inner lead by anode plate junction.

[Claim 19] The manufacture approach of the electronic parts which will adhere the insulating coat which becomes conductivity if it heats around the bump who prepared in the polar zone of a semiconductor chip, carry out anode plate junction of said insulating coat and inner lead after laying the bump of said polar zone in the inner lead formed in the flexible tape for TAB automatic mounting of etching, and are characterized by connecting said electrode to an inner lead electrically through said bump.

[Claim 20] if it heats on the base of a semiconductor device in which the ball grid array for external wiring was prepared, after a part of crowning of said ball grid array will adhere the insulating coat which becomes conductivity to extent exposed — said ball grid array — wiring on the circuit board — a conductor — laying — said insulating coat and said wiring — carrying out anode plate junction of the conductor — said ball grid array and wiring — the manufacture approach of the electronic parts characterized by to connect a conductor electrically.

[Translation done.]

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DETAILED DESCRIPTION

[Detailed Description of the Invention]

[0001]

[Industrial Application] the conductor of the insulating layer which surrounds the polar zone on the front face of a semiconductor chip in case each electrode of a semiconductor chip boils this invention especially, respectively, it carries out the coincidence pressure welding of the wiring for external drawers about the manufacture approach of of the electronic parts and electronic parts which were manufactured using the anode plate conjugation method and it connects, and wiring for external drawers — it is made to connect with wiring for external drawers, and the polar zone electrically by carrying out anode plate junction of the front face

[0002]

[Description of the Prior Art] Drawing 39 is the perspective view showing the condition of having connected electrically the electrode 2 prepared in the front face of a semiconductor chip 1 by the conventional ultrasonic thermocompression bonding type wire bond method, and the inner lead 4 extended from the leadframe which is not illustrated by the gold streak 5. Drawing 40 is drawing which modeled the situation when performing ultrasonic thermocompression bonding for the end of a gold streak 5 to the electrode 2 prepared in the front face of a semiconductor chip 1.

[0003] In drawing 40, the base plate which 41 is a die pad and supports a semiconductor chip 1, and 6 show the die bond material for fixing a semiconductor chip 1 to a die pad 41. The purpose of the die bond material 6 and a die pad 41 supports a chip 1 while supporting the thrust of the capillary tube 7

which becomes the ball bonding configuration shown in 52, when carrying out ultrasonic thermocompression bonding of the ball 51 at the tip of a gold streak 5 to an electrode 2.

[0004] In an ultrasonic thermocompression bonding type wire bond method, after the tip of the gold streak 5 which penetrated the inside of a capillary tube 7 has come out from the tip of a capillary tube 7, a ball 51 is formed at the tip of a gold streak 5 of high-pressure discharge. Then, a ball 51 is that are pressed by the electrode 2 prepared on the semiconductor chip 1, and supersonic vibration and heat are impressed, and as shown in 52 of this drawing, ultrasonic thermocompression bonding of the ball 51 is carried out to an electrode 2. And after a capillary tube 7 moves to the location of the point of an inner lead 4, it drops a capillary tube 7 and connects the point and gold streak 5 of an inner lead 4.

[0005] (a), (b), and drawing 42 of drawing 41 are drawing showing the structure of the leadframe when connecting the tip of an inner lead 4 with an electrode 2 by the gold streak 5 by the conventional ultrasonic thermocompression bonding wirebonding method, and the framework 3 shows that from which eight die pads 41 which are not illustrated and inner leads 4 constituted addressing to 36 piece in one in (a) of drawing 41 .

[0006] (b) of drawing 41 shows drawing which expanded the "A" part of this drawing (a). In this drawing, 3 shows the framework and 4 shows one of the representation of the 36 inner leads. It prepared in order for 41 to support a die pad 41 with a die pad and for 42 to support with the framework 3, and it hangs, and a lead is shown. 44 shows the part used as an external lead.

[0007] Drawing 42 is 36 inner leads 4, a die pad 41, and drawing in which hanging and showing the detail of lead 42. The rectangle shown with an alternate long and short dash line in this drawing shows the location by which sheathing is carried out by mold resin. Drawing 43 is the conventional ultrasonic thermocompression bonding wire bond method explained above, and after it connects an inner lead 4 with an electrode 2 by the gold streak 5, it shows the sectional view of the semiconductor device which carried out the sheathing mold of the framework 3 by mold resin 8, and was completed. In this drawing, 53 shows the connection part after carrying out ultrasonic thermocompression bonding of the gold streak 5 and inner lead 4 which were explained by drawing 40 .

[0008] Drawing 44 shows drawing which expanded the part which stuck the gold streak 5 to the electrode (not shown) and inner lead 4 on a chip 1 by pressure. Drawing 45 is the detail drawing showing the situation of deformation of the ball 51 when carrying out ultrasonic thermocompression bonding of the ball 51, and completing in the electrode 2 prepared in the front face of a semiconductor chip 1. In this drawing, although a gold streak 5 and the ball variant part 52 are the golden stroke material itself when an electrode 2 is used as an aluminum electrode, and ultrasonic thermocompression bonding is completed, the alloy layer of gold and aluminum is formed in the part of 54. 2i shows the electric insulation passivation film (it is hereafter indicated as an electric insulator layer) to which the electrode 2 was avoided and it adhered on the semiconductor chip 1.

[0009] Drawing 46 shows the condition that the ball variant part 52 of a gold streak 5 was pressed by the electrode 2 by the capillary tube 7, and connection was completed. Stitch bonding of the other end of a gold streak 5 is carried out to an inner lead 4 by the capillary tube 7, and drawing 47 shows the condition that a part for the variant part 53 was pressed by the amount of [of an inner lead 4] point. In drawing 47 , although the golden alloy layer 54 arises like drawing 45 since silver plating will be carried out at the time of an iron frame although a stitch side changes with lead frame material if stitch bonding of the inner lead 4 is carried out to a part for a variant part 53, and the alloy layer of gold and silver arises, the alloy layer 54 is omitted in this Fig.

[0010] (a) - (e) of drawing 48 explains the process which connects the electrode and inner lead 4 on a semiconductor chip 1 by the gold streak 5 with the conventional ultrasonic thermocompression bonding wire bond. In drawing 48 (a), supply of heat is told to a chip 1 by heat conduction through a die pad 41 from the heat block 9. The tip of the gold streak 5 drawn from the tip of a capillary tube 7 is cast by the ball on the high-voltage-power-supply torch 10.

[0011] This drawing (b) drops a capillary tube 7 to an electrode 2 (it omits in this Fig.), and shows the

condition of having stuck the cast ball 51 to the electrode 2 by pressure by supersonic vibration and thrust. This drawing (c) shows the condition of moving the capillary tube 7 which let the gold streak 5 pass to an inner lead 4 in order to connect the other end of a gold streak 5 to an inner lead 4, after the ultrasonic thermocompression bonding of a ball 51 is completed, as shown in drawing 45 . This drawing (d) shows the condition of having made stitch bonding the inner lead 4 for the other end of a gold streak 5. after the other end of a gold streak 5 is stuck to an inner lead 4 by pressure by stitch bonding in the condition which shows this drawing (e) in drawing 47 , a capillary tube 7 is **** in a clamp 11 about a gold streak 5 — it pulls up in the condition and the condition of having cut the gold streak 5 in the stitch-bonding part is shown.

[0012] Drawing 49 shows the top view which looked at the semiconductor chip 1 after connecting between an electrode 2 and inner leads 4 by the gold streak 5 from the top face by ultrasonic thermocompression bonding. Drawing 50 shows drawing where 19 electrodes 2 have been arranged on a semiconductor chip 1, and 2i shows the electric insulator layer to which it adhered by continuing throughout removing an electrode 2 on the front face of a semiconductor chip 1.

[0013] An electrode 2 consists of area shown in a C dimension xE dimension, and opening of the electric insulator layer 2i is carried out with the dimension B dimension xD dimension exceeding the area of an electrode 2, and it is making the electrode 2 expose from electric insulator layer 2i, as the boundary of electric insulator layer 2i and an electrode 2 is shown in drawing 51 . As the configuration of the tomographic layer of a semiconductor chip 1 is shown in drawing 45 , electric insulator layer 2i has lapped with the periphery of an electrode 2. As shown in drawing 51 , the area of an electrode 2 must be larger than electric and the peripheral face product of the ball variant part 52 in order to raise mechanical degree of coupling, when ultrasonic thermocompression bonding of the ball 51 is carried out of a gold streak 5.

[0014] Moreover, the dimension a of the center to center of each electrode 2 shown in drawing 51 with the precision of wire bond equipment must be decided in consideration of the periphery dimension of the ball variant part 52 etc. In the limitation which generally carries out ultrasonic thermocompression bonding, the electrode 2 for carrying out wire bond must enlarge width of face as compared with the width of face of the circuit wiring 21 shown in this drawing. Moreover, as shown in drawing 52 , it must be careful of I dimension, J dimension, K dimension, and L dimension to be the conventional wire bond approach, and the semiconductor device which considered the precision of a wire bonder and the engine performance must be designed.

[0015] Drawing 53 shows the sectional view when cutting on the axis with which wiring of the gold streak 5 shown with the top view of drawing 52 was continued and carried out to the electrode 2 and the inner lead 4. It checks whether the dimension to the corner of the semiconductor chip 1 of a gold streak 5 can be taken enough with checking I dimension. The clearance between the corner of a die pad 41 and a gold streak 5 is checked from the relation between J dimension, a die pad 41, and an inner lead 4. Moreover, it is necessary to check with K dimension whether sufficient dimension for stitch-bonding 53 part is secured.

[0016] (a) of drawing 54 is the perspective view showing the internal structure of the semiconductor device (integrated circuit) which connected the electrode 2 and inner lead 4 which have been arranged in the center section of the chip 1 by the gold streak 5 using the ultrasonic thermocompression bonding wire bond method, and was completed. (b) of this drawing is a sectional view at the time of cutting by part for the II line part of this drawing (a). (a) of drawing 55 shows the sectional view of the TAB package currently performed conventionally. In this drawing, 21 is an electrode bump, and the electrode bump 21 is beforehand formed in tape career electrode lead (it is hereafter indicated as electrode lead) 4b by thermocompression bonding. (b) of this drawing is the enlarged drawing expanding and showing the connection part of the electrode bump 21 and an electrode. In a TAB method, the electric junction to an electrode and electrode lead 4a is made by making connection between the electrode of a semiconductor chip 1, and electrode lead 4a through the electrode bump 21.

[0017] Drawing 56 shows drawing which illustrated the approach of carrying out anode plate junction of the semiconductor material which was shown in JP,53-28747,B, and which becomes with silicon at electric insulation material. In drawing 56 , 1a is a semiconductor material and this semiconductor material 1a is laid in the resistance heating strip 67 which energizes according to a power source A and is radiating heat. 1b is glass membrane (for example, boro-silicated glass which used a boric acid and silicic acid as the component) which is an insulating coat which will serve as conductivity slightly if the front face of semiconductor material 1a adheres and it heats. The electric insulating material from which 68 becomes the candidate for junction laid on top of semiconductor material 1a through insulating coat 1b, and 65 are pieces of pressure connection which make the front face of semiconductor material 1a press the electric insulating material 68 lightly. In addition, 60 is the DC power supply for passing a forward current from semiconductor material 1a to the electric insulating material 68. The positive-electrode terminal 63 of DC power supply 60 is connected to the resistance heating strip 67, and the negative-electrode terminal is connected to the piece 65 of pressure connection.

[0018] Next, the anode plate junction approach is explained. It heats until semiconductor material 1a is slightly electrified by insulating coat 1b through the resistance heating strip 67 (about 400 degrees - 700 degrees of this heating temperature change with insulating coat material). Consequently, by energizing few forward currents (for example, severalmicroA/mm 2) from semiconductor material 1a to the electric insulating material 68 for about 1 minute, an anode plate growth oxide joint is formed in the interface of semiconductor material 1a and the electric electric insulating plate 68, and anode plate junction of semiconductor material 1a and the electric insulating material 68 is carried out.

[0019] At this time, the electric insulating material 68 is dissolved by neither heating temperature nor force current. Heating only makes the operation which only makes insulating coat 1b conductivity. Junction of semiconductor material 1a and the electric insulating material 68 can be accomplished from semiconductor material 1a only by leading a forward current to the electric insulating material 68.

[0020] Drawing 57 shows drawing which illustrated ****** which sets two semiconductor materials 1c and 1d which were similarly shown in JP,53-28747,B, and which become with silicon by anode plate junction by the electrical insulation material material 68. In this approach, after laying two semiconductor materials 1c and 1d which adhered insulating coat 1b to the plane of composition in the electric insulating material 68, this electric insulating material 68 is laid in a resistance heating strip. In addition, each semiconductor materials 1c and 1d have DC power supplies 61 and 62 for passing a forward current separately, a positive-electrode terminal is connected to the semiconductor materials 1c and 1d corresponding to each DC power supplies 61 and 62, and common connection of each negative-electrode terminal is made at the resistance heating strip 67.

[0021] Next, the anode plate junction approach is explained. It heats until semiconductor materials 1c and 1d are slightly electrified by insulating coat 1b through the electric insulating material 68 from the resistance heating strip 67. Consequently, by energizing few forward currents (for example, severalmicroA/mm 2) from semiconductor materials 1c and 1d to the electric insulating material 68 for about 1 minute, an anode plate growth oxide joint is formed in the interface of semiconductor materials 1c and 1d and the electric electric insulating plate 68, and anode plate junction of semiconductor materials 1a and 1d and the electric insulating material 68 is carried out.

[0022] As an example of general use of the anode plate electrode junction approach indicated by other official reports, the silicon front face of the rear face of a silicon wafer is used as a conductor front face at JP,1-185242,B and JP,4-164841,B, and how to connect between this conductor front face and the front faces of a glass wafer is shown. JP,53-28747,B shows the example which joins a sapphire insulating material etc. to junction to silicon and a quartz, junction to the boro-silicated glass which is heat-resisting glass with the small expansion coefficient which used silicon, a boric acid, and silicic acid as the component, the junction to a germanium semi-conductor and boro-silicated glass, and silicon as a semi-conductor.

[0023] Moreover, the approach of carrying out anode plate junction of a silicon wafer and the silicon

base material wafer in a capacity mold pressure sensor is shown in JP,63-117233,B as a special application. Since the principle of an anode plate conjugation method is shown in JP,53-28747,B etc., explanation of the detail of anode plate junction is omitted.
[0024] Drawing 58 shows the top view of the conventional laminating multilayer insulating substrate. Drawing 59 shows the cross-section perspective view showing the vertical structure. In drawing 58 , 70 is wiring with which a laminating multilayer insulating substrate and 71 were carried out at the electric insulating plate, and pattern NINGU of 76 was carried out on the electric insulating plate 71. Moreover, in drawing 59 , the electric insulating plate of five sheets with which the laminating of 71-75 was carried out, 76-81, and the part smeared away black are wiring by which pattern NINGU was carried out on each electric insulating plate 71-75. Wiring and the flow of each insulating substrates 71-75 by which a laminating is carried out to the through hole established in insulating substrates 71-75 for carry out the laminating of each insulations 71-75 and creating the laminating multilayer insulating substrate 70 through lead wire were taken. [0025] Although the wire bond method was first explained by the junction approach in the conventional technique, the bump conjugation method by TAB was subsequently explained and the anode plate junction approach was finally described, using an anode plate conjugation method, when joining the plinth which uses a chip front face with an insulating coat a wrap case and for the stress relaxation in a pressure sensor, and the silicon which forms a strain gauge is known.
[0026] the silicon itself which joins the anode plate conjugation method generally used conventionally to a glass electric insulating plate — it is used for joining that in which it has a certain amount of rigidity, and a glass electric insulating plate also has rigidity comparable as silicon.
[0027] the above explanation — the wire bond method — 1. ball formation Heating in 2. supersonic-wave thermocompression bonding, thrust impression, and supersonic vibration supply 3. capillary tube migration Ultrasonic thermocompression bonding of 4. stitch section 5. — a gold streak — if it is addressing line trap ****** to one inner lead about five processes of cutting, there is nothing.
[0028] It also sets to the bump junction by TAB, and is 1. heating sticking by pressure. Only the number of electrode junction prepared on the chip needs to repeat the process of 2. migration. Current utilization of the package bonding is not carried out.
[0029] As for these junction approaches, all join a metallic conductor comrade by ultrasonic thermocompression bonding or thermocompression bonding to the electrode which should carry out electrical installation, and an electrode, i.e., a metallic conductor. Therefore, the mechanical strength for the joint which performs electrical installation, for example, shear strength, will be decided by the condition of a joint.
[0030] Moreover, ultrasonic thermocompression bonding or the part which carried out thermocompression bonding is what carried out lifting recombination for destruction to the metallic contact frictional heat systematically by the strong sexual impression load, and constituted the alloy layer. Therefore, safe reinforcement is not securable if a plane-of-composition product is not enlarged. For example, things with a diameter [of a gold streak] of phi= 25 micrometers are the diameter of phi= 100 micrometers of a joint adhesion side, and 4 times the diameter of a golden wire size, and area has become 16 times.
[0031]
[Problem(s) to be Solved by the Invention] There were the following troubles in the connection method of the electrode and inner lead in the conventional semiconductor device.
(b) Learn, if mechanical reinforcement is not secured by part for the both ends of the gold streak which makes connection between the conventional inner lead and an electrode for electrical installation by the approach of performing through a rigid weak member very much like a gold streak, and it is **. Therefore, in order to secure mechanical reinforcement, it is necessary to secure the dimension of a connection part too much than a dimension required for electrical installation. Consequently, it must be contrary to the densification purpose of an integrated circuit (IC), the dimension of the electrode on a chip must be enlarged, and the miniaturization of IC chip will be checked.

[0032] (b) moreover, a part for the both ends of the gold streak which makes connection between the conventional inner lead and an electrode for electrical installation by the approach of performing through a rigid weak member very much like a gold streak and a gold streak — as for carrying out the mold of a semiconductor chip and the inner lead in order to protect the purpose and the semiconductor chip itself etc. which protects the very thing from an external load from an external environment, the dimension of a semiconductor device had the trouble that it could not become predetermined magnitude, inevitable therefore.

[0033] (c) By high integration of the latest IC, the number of the electrodes which take out a signal outside has increased. However, it learns, if the dimension of an electrode is not decided to be a predetermined dimension in the bump continuation by the conventional wire bond method or TAB in order to secure mechanical bonding strength to some extent, and it is **. As the result, the dimension of the whole chip will be influenced by the number of electrodes, and will check the miniaturization of IC chip.

[0034] (d) If an inner lead is installed in the exterior of the closure section and the number of formation ********** becomes 1000 or more-pin many pins, even if dispersion arises for connection precision that they are one electrode and the wire bond conjugation method which performs a junction activity to one, verification of whether junction to an electrode is performed normally will become difficult.

[0035] (e) Grasp of the exact value of the mechanical strength of the alloy layer made by the joint especially by ultrasonic thermocompression bonding or thermocompression bonding must expect a high safety factor from a difficult thing, and must design a joint. Therefore, an erector has to do vibration produced in inside, a self-weight, and the design which is generous enough in consideration of other external force, and will receive a design-limit.

[0036] (**) the conventional electrode connection method — connection actuation — several n of an electrode — corresponding — n times or twice many 2n [as this] time — it needed to repeat. Therefore, the more it becomes the semiconductor device of a multi-pin configuration, the more the time amount which connection takes increases.

[0037] This invention was made in order to cancel the above troubles, and mechanical association with the insulator layer electric connection and an inner lead, and around an electrode an inner lead and an electrode is firm, and it aims at acquiring the manufacture approach of of the electronic parts and electronic parts which can use an anode plate conjugation method for each of two or more electrodes, can bundle up an inner lead to it, and can moreover carry out bonding to it.

[0038]

[Means for Solving the Problem] The electronic parts manufactured using the anode plate conjugation method concerning invention of claim 1 It has a circuit element with the electrode electrically connected with the conductor for current I/O. If it heats around said electrode, after adhering the insulating coat which becomes conductivity, said conductor is contacted to said electrode, anode plate junction of the insulating coat and said conductor of a superposition lever is carried out on said insulating coat, and said conductor and said electrode are connected electrically.

[0039] If the electronic parts which manufactured using the anode plate conjugation method concerning invention of claim 2 heat on the surface of a semiconductor chip, they avoid the electrode in which the insulating coat which becomes conductivity was prepared on said semiconductor chip front face, will adhere, and they connect this inner lead and electrode electrically while they carry out the anode plate junction of the tip of this insulating coat and said inner lead where the tip of the inner lead installed from the leadframe is put on said insulating coat so that this electrode may cover.

[0040] The electronic parts manufactured using the anode plate conjugation method concerning invention of claim 3 adhere a metal coat on the insulating passivation film prepared in the front face of a semiconductor chip according to claim 2.

[0041] The electronic parts manufactured using the anode plate conjugation method concerning invention of claim 4 make the front face of the electrode on a semiconductor chip according to claim 2

higher than the maximum top face of the insulating coat which will become conductivity if it heats to which the front face of said semiconductor chip adhered.

[0042] The electronic parts manufactured using the anode plate conjugation method concerning invention of claim 5 make a convex configuration the tip configuration of an electrode according to claim 4.

[0043] The electronic parts manufactured using the anode plate conjugation method concerning invention of claim 6 constitute the front face of the electrode on a semiconductor chip according to claim 2 so that it may become lower than the maximum top face of the insulating coat which will become conductivity if it heats to which the front face of said semiconductor chip adhered.

[0044] The electronic parts manufactured using the anode plate conjugation method concerning invention of claim 7 lay the conductive matter with a small elastic modulus with which a part projects from the front face of said insulating coat in the electrode prepared in the field lower than the front face of the insulating coat according to claim 5 which will become conductivity if it heats.

[0045] The electronic parts manufactured using the anode plate conjugation method concerning invention of claim 8 use mercury for the conductive matter according to claim 7.

[0046] the insulating coat which will become conductivity if the electronic parts manufactured using the anode plate conjugation method concerning invention of claim 9 are heated on a part of front face of the inner lead by which anode plate junction was carried out on the semiconductor chip according to claim 2 -- adhering -- wiring of the circuit board -- a conductor -- laying -- said insulating coat and wiring -- anode plate junction of the conductor is carried out.

[0047] The electronic parts manufactured using the anode plate conjugation method concerning invention of claim 10 make the end of the inner lead by which anode plate junction was carried out on the semiconductor chip according to claim 2 refracted as edge ** of said semiconductor chip, and are cast to an out lead.

[0048] The electronic parts manufactured using the anode plate conjugation method concerning invention of claim 11 If it heats on the surface of a semiconductor chip, while avoiding the electrode in which the insulating coat which becomes conductivity was prepared on said semiconductor chip front face and adhering wiring electrically joined to said electrode -- a conductor -- the conductor which contacts except with said insulating coat -- the circuit board which made the piece pattern NINGU -- said semiconductor chip -- mounting -- said insulating coat and conductor -- carrying out anode plate junction of the piece -- said electrode and wiring -- electric junction of the conductor is carried out.

[0049] The electronic parts manufactured using the anode plate conjugation method concerning invention of claim 12 The insulating coat which will become conductivity if it heats to a piece is adhered. wiring by which patterning was carried out to the 1st circuit board -- the conductor by which was insulated from the conductor and patterning was carried out -- said wiring -- a conductor and wiring which takes electrical installation -- a conductor and this wiring -- the conductor insulated from the conductor -- the 2nd circuit board to which patterning of the piece was carried out -- said 1st circuit board -- a laminating -- carrying out -- said insulating coat and conductor -- anode plate junction of the piece is carried out, and the laminating circuit board is formed.

[0050] the electronic parts manufactured using the anode plate conjugation method concerning invention of claim 13 -- wiring of an out lead of a semiconductor device -- a conductor -- the insulating coat which will become conductivity if it heats in a part of contact section -- adhering -- wiring of the circuit board -- a conductor -- arranging -- this insulating coat and wiring -- a semiconductor device is made to mount in the circuit board in carrying out anode plate junction of the conductor, and it is a thing.

[0051] The electronic parts manufactured using the anode plate conjugation method concerning invention of claim 14 The insulating coat which will become conductivity if it heats around this height while preparing a height at the tip of an inner lead is adhered. Form the crevice which adheres a metallic film to the perimeter of the electrode on said semiconductor chip by predetermined thickness, and

reaches said electrode, said height is made to engage with this crevice, said inner lead and said electrode are contacted, and anode plate junction of said insulating coat and said metallic film is carried out.

[0052] If it is adhered at the tip of an inner lead to the electronic parts manufactured using the anode plate conjugation method concerning invention of claim 15 and they heat, they prepare opening which reaches an inner lead in the insulating coat which becomes conductivity, will form a crevice, and where made the convex electrode projected and prepared in this crevice from the metallic film on said front face of a semiconductor chip engaged and said inner lead and said electrode are contacted, they carry out the anode plate junction of said insulating coat and said metallic film.

[0053] If the electronic parts manufactured using the anode plate conjugation method concerning invention of claim 16 are heated at the rear face of a semiconductor chip, after they will adhere and will lay the insulating coat which becomes conductivity in the die pad of a leadframe, they carry out anode plate junction of said insulating coat and die pad, and fix said leadframe pad to said semiconductor chip.

[0054] If the manufacture approach of the electronic parts concerning invention of claim 17 is heated on all the front faces except an electrode, after it will adhere the insulating coat which becomes conductivity to the front face of a semiconductor chip, it carries out alignment of the part for the point of each inner lead to the top face of an electrode, and it connects said each electrode and inner lead to coincidence electrically in the process which joins said each inner lead and said insulating coat with an anode plate conjugation method.

[0055] The manufacture approach of the electronic parts concerning invention of claim 18 On the front face of each semiconductor chip which carried out division separation and formed the semi-conductor wafer in plurality If it heats by all the front faces except an electrode adhering, in case the insulating coat and inner lead which become conductivity will be joined with an anode plate conjugation method After fitting into the crevice established in said insulating coat layer and inserting the conductive matter with a small elastic modulus in an electrode, Said inner lead and said electrode are connected electrically, carrying out the pressure welding of said conductive matter to said electrode in the process which carries out anode plate junction of said insulating coat and said inner lead by anode plate junction.

[0056] If the manufacture approach of the electronic parts concerning invention of claim 19 is heated around the bump who prepared in the polar zone of a semiconductor chip, it will adhere the insulating coat which becomes conductivity, after it lays the bump of said polar zone in the inner lead formed in the flexible tape for TAB automatic mounting of etching, it carries out anode plate junction of said insulating coat and inner lead, and it connects said electrode to an inner lead electrically through said bump.

[0057] if the manufacture approach of the electronic parts concerning invention of claim 20 heats to extent which the crowning of said ball grid array exposes to the base of a semiconductor device in which the ball grid array for external wiring was prepared, after it will adhere the insulating coat which becomes conductivity — said ball grid array — wiring on the circuit board — a conductor — laying — said insulating coat and said wiring — carrying out the anode plate junction of the conductor — said ball grid array and wiring — a conductor makes connect electrically

[0058]

[Function] The electronic parts manufactured using the anode plate conjugation method in invention of claim 1 are carrying out anode plate junction of a conductor and the insulating coat of the perimeter of an electrode, and they can make high whenever [over the electrode of a conductor / electric junction] while being able to join to a circuit element firmly mechanically, without fusing a conductor.

[0059] The electronic parts manufactured using the anode plate conjugation method in invention of claim 2 are carrying out anode plate junction of the part for the point of the inner lead installed from the leadframe at the insulating coat around the electrode of a semiconductor chip, and they can make high whenever [over the electrode of an inner lead / electric junction] while they can join an inner lead firmly mechanically on a semiconductor chip.

[0060] Since the maximum top face of a semiconductor chip adheres to **********, they stop being influenced of an electromagnetic wave etc. easily, while they can carry out anode plate junction by making a semiconductor chip into an anode plate at a wiring substrate, since the electronic parts manufactured using the anode plate conjugation method in invention of claim 3 prepared the metallic film on the insulating passivation film of a semiconductor chip.

[0061] The electronic parts manufactured using the anode plate conjugation method in invention of claim 4 are having made the front face of an electrode established in the top face of a semiconductor chip project from the front face of the insulating coat adhering to a perimeter, and whenever [to the inner lead by which anode plate junction is carried out with an insulating coat / electric junction] becomes high.

[0062] When the crowning of the electrode which prepared the electronic parts manufactured using the anode plate conjugation method in invention of claim 5 in the top face of a semiconductor chip, and was made to project from the front face of the adhering insulating coat was made convex and anode plate junction of an inner lead and the insulating coat is carried out, as for the crowning of an electrode, an inner lead becomes is easy to be crushed, and it becomes easy [top height adjustment] while electric junction increases.

[0063] The electronic parts manufactured using the anode plate conjugation method in invention of claim 6 are having made the front face of the electrode on a semiconductor chip lower than the front face of the insulating coat adhering to a perimeter, and having formed the crevice, and can lay the conductive matter which can ensure a flow with an inner lead and an electrode in a crevice.

[0064] Whenever [flow-with electrode and inner lead] improves more the conductive matter which the electronic parts manufactured using the anode plate conjugation method in invention of claim 7 are laid in an electrode, and is pressed by the inner lead through the conductive matter by the thing with a small elastic modulus to do for the matter.

[0065] The electronic parts manufactured using the anode plate conjugation method in invention of claim 8 are making into a mercury bulb the conductive matter which is laid in an electrode and pressed by the inner lead, and, as for a touch area with mercury, an inner lead, and an electrode, flow-with breadth electrode and inner lead whenever improve at the time of compression of a mercury bulb.

[0066] a part of front face of the inner lead which anode plate junction of the electronic parts manufactured using the anode plate conjugation method in invention of claim 9 was carried out on the semiconductor chip, and was electrically joined to the electrode -- an insulating coat -- adhering -- wiring of the circuit board -- even if it does not pull out an external connection lead from a semiconductor chip by carrying out anode plate junction with a conductor, ************** can be mounted in the circuit board.

[0067] The electronic parts manufactured using the anode plate conjugation method in invention of claim 10 can manufacture the semiconductor device which miniaturized the whole by it being caudad refracted along with the edge of a semiconductor chip, and considering the end of the inner lead which carried out anode plate junction as an external connection lead on a semiconductor chip.

[0068] wiring to which an electrode is joined to the insulating coat with which the electronic parts manufactured using the anode plate conjugation method in invention of claim 11 adhered to the perimeter of the electrode of a semiconductor chip -- a conductor -- a surrounding conductor -- firm in mechanical junction of as opposed to the circuit board of a semiconductor chip by carrying out anode plate junction of the piece -- while carrying out a thing -- an electrode and wiring -- electric junction to a conductor can be performed firmly.

[0069] The electronic parts manufactured using the anode plate conjugation method in invention of claim 12 An insulating coat is adhered to a piece. wiring by which patterning was carried out to the 1st circuit board -- a conductor -- the conductor of an except -- wiring of the 2nd circuit board -- a conductor and this wiring -- a conductor -- the conductor of an except -- wiring of a piece and the 1st circuit board -- a conductor and a conductor -- a laminating wiring substrate with high thickness

dimensional accuracy can be created by piling up a piece, carrying out anode plate junction, and making a multilayer laminating wiring substrate.
[0070] the electronic parts manufactured using the anode plate conjugation method in invention of claim 13 — wiring of an out lead of a semiconductor device — a conductor — a part of contact section — an insulating coat — adhering — wiring of the circuit board — a conductor — after arranging upwards — an insulating coat and wiring — two or more semiconductor devices by ** which carries out anode plate junction of the conductor can be mounted in a wiring substrate at coincidence.
[0071] It is making the crevice which carried out opening engaged and carrying out anode plate junction with an inner lead and an insulating coat until the electronic parts manufactured using the anode plate conjugation method in invention of claim 14 result the insulating coat on a height and the front face of a semiconductor chip in an electrode as having formed in the point of an inner lead, and association with an inner lead and an electrode becomes firm.
[0072] The electronic parts manufactured using the anode plate conjugation method in invention of claim 15 are making the crevice which carried out opening of the insulating coat adhering to the point of an inner lead, and formed it, and the convex electrode projected from the metallic film to which it adhered on the semiconductor chip engaged, and carrying out anode plate junction of an insulating coat and the metallic film, and association with an inner lead and an electrode becomes firm.
[0073] The electronic parts manufactured using the anode plate conjugation method in invention of claim 16 adhere an insulating coat to the rear face of a semiconductor chip, and they are carrying out anode plate junction at the die pad of a leadframe, and carrying out anode plate junction of the inner lead on a semiconductor chip, and die bond material becomes unnecessary and they can manufacture a semiconductor device cheaply.
[0074] After the manufacture approach of the electronic parts in invention of claim 17 adheres an insulating coat to the perimeter of each electrode prepared on the semiconductor chip front face, it is carrying out anode plate junction of the inner lead which positions the point of each inner lead from a leadframe towards a corresponding electrode, and corresponds with each electrode collectively, and while each inner lead is mechanically combined with a semiconductor chip firmly in the large range, an inner lead and an electrode are joined electrically.
[0075] Whenever [to an inner lead and an electrode / touch-area and junction] improves with the conductive matter by laying the conductive matter which will be deformed plastically if the manufacture approach of the electronic parts in invention of claim 18 is pressed by the part of an electrode by the inner lead.
[0076] The manufacture approach of the electronic parts in invention of claim 19 positions the tip of each inner lead etched into the flexible tape of TAB automatic mounting to the bump who prepared in each electrode on a semiconductor chip, and can join a semiconductor chip to an inner lead at few processes as compared with the TAB automatic mounting conventional by carrying out anode plate junction of each INA lead and the insulating coat which adhered on the semiconductor chip.
[0077] wiring with which a ball grid array contacts the insulating coat to which, as for the manufacture approach of the electronic parts in invention of claim 20, the ball grid array adhered, so that the crowning of a ball grid array was exposed to the base of **** eclipse ************ — carrying out anode plate junction of the conductor — it is — the process of anode plate junction — a ball grid array and wiring — since a conductor is joined electrically, even if it is the semiconductor device of a multi-pin configuration, it can mount in a wiring substrate at few processes in a short time.
[0078]
[Example]
One example of this invention is explained about drawing below example 1. Drawing 1 is a side-face sectional view of an anode plate junction means and a semiconductor chip which explains how to carry out anode plate junction of the inner lead to each electrode of a semiconductor chip. ****** — it is electrified by the part heated when 1 is a semiconductor chip and an insulating coat with which 2a

becomes the front face of a semiconductor chip 1 by the glass material which avoided the part of an electrode and adhered it by the sputtering approach and heated.

[0079] The boro-silicated glass (generally used for a flask etc.) which uses a boric acid and silicic acid as a component as the quality of the material of glass material is desirable. That is because the coefficient of linear expansion of boro-silicated glass is almost equal to the coefficient of linear expansion of the electric insulator layer which consists of the silicon oxide on a semiconductor chip 1, so it is hard to exfoliate from an electric insulator layer even if an insulating coat gets cold.

[0080] 3 is the leadframe which carried out the configuration as shown in drawing 42 . But, in the leadframe 3 in this example, the die pad 41 needed for laying a semiconductor chip conventionally, and since direct anode plate junction of the inner lead 4 will be carried out with a semiconductor chip 1 if it hangs and lead 42 (an alternate long and short dash line shows) uses the anode plate junction approach, it becomes unnecessary. In addition, a semiconductor chip 1 is positioned by the central part of the location in which the conventional die pad 41 was formed in drawing 1 . And each inner lead 4 is extended to right above [of each electrode of a semiconductor chip 1], as shown in drawing 3 .

[0081] Moreover, in drawing 3 , the part which an alternate long and short dash line is the location at the tip of the conventional inner lead 4, and was lengthened ahead of the alternate long and short dash line shows inner lead 4a by this example. The tip of inner lead 4a is extended over the electrode 2 formed in the top face of a semiconductor chip 1. in this drawing, while anode plate junction of the part for the point of inner lead 4a smeared away black is carried out with insulating coat 2a on a semiconductor chip 1, both electrical installation should line-do by pressing an electrode 2 with the rear face of in NARI 4a -- **. That is, if it is joined to insulating coat 2a and inner lead 4a goes, the plane of composition of inner lead 4a will press on the front face of the electrode 2 projected from insulating coat 2a in the several microns unit, and electrical installation will be made.

[0082] 60 shows DC power supply and 63 shows the anode terminal of DC power supply 60, and a resistance heating plate and the power lead to which a pressure contact segment and 67 are energized from 66a to the resistance heating plate 67, and 64 energizes 66b for the cathode terminal of DC power supply 60, and 65 from a power source A. This configuration is the same as the configuration shown in drawing 58 . When 68a carries out anode plate junction of a semiconductor chip 1 and the leadframe 3, the piece of a metal which is the positioning fixture which makes exact positioning of the purpose and semiconductor chip 1 which ensure contact to insulating coat 2a and the plane of composition of a leadframe 3, the power lead by which 69 applies forward potential to a leadframe 3 from DC power supply 60, and 70 are power leads which apply negative potential to a semiconductor chip 1 through the pressure contact segment 65 from DC power supply 60.

[0083] When a power source A acts to the resistance heating plate 67 as Nagare of the current through a power lead 66, the resistance heating plate 67 radiates heat, heats insulating coat 2a at 400 degrees C about **50 degrees C through a leadframe 3, and makes it electrified by the above configuration. If direct current voltage is impressed from DC power supply 60 between a leadframe 3 and positioning fixture 68a in the condition of having been electrified, a forward current will flow between insulating coat 2a and a leadframe 3. Consequently, electrostatic adhesive strength and electrochemistry bonding strength occur in the interface two a1 (the thick wire of the lower part of insulating coat 2a shows) of insulating coat 2a and a leadframe 3, and anode plate junction of the inner lead and semiconductor chip front face at leadframe 3 tip is carried out.

[0084] moreover, as shown in drawing 3 , while anode plate junction of the part for the point of inner lead 4a smeared away black is carried out with insulating coat 2a on a semiconductor chip 1 in this drawing about the electrical installation of an inner lead 3 and the electrode of a semiconductor chip 1, both electrical installation should line-do by pressing an electrode 2 with the rear face of in NARI 4a -- **. That is, if it is joined to insulating coat 2a and inner lead 4a goes, the plane of composition of inner lead 4a will press on the front face of the electrode 2 projected from insulating coat 2a in the several microns unit, and electrical installation will be made.

[0085] Drawing 2 is drawing which explains an example of the approach of carrying out anode plate junction of two or more semiconductor chips 1 at coincidence to an inner lead 3. In this drawing, DC power supply for 61 to pass a forward current to insulating coat 2a of one semiconductor chip 1 and a leadframe 3 and 62 show the DC power supply for passing a forward current to insulating coat 2a of the semiconductor chip 1 of another side, and a leadframe 3. When putting two semiconductor chips 1 and 1 on a leadframe 3 and carrying out anode plate junction at coincidence, he is trying to pass a forward current between each semiconductor chips 1 and 1 and a leadframe 3 in drawing using two DC power supplies 61 and 62. in this case, if positioning of the semiconductor chips 1 and 1 to a leadframe 3 is correctly made with a certain means, it is shown in drawing 1 — as — pressing down — a common [a positioning / a fixture-cum-/ fixture-cum-] short circuit — a conductor — there is no need of using positioning fixture 68a as a piece.

[0086] And what is necessary is to only use the insulating coat 2a side as cathode, in order to carry out anode plate junction, and just to pass a forward current by this approach, by making into an anode plate the leadframe 3 which is a metallic conductor. Moreover, forward potential may be impressed from each DC power supply so that the single or two or more collets (vacuum adsorber) which adsorb a leadframe 3 and which are not illustrated may serve as an anode plate. In this case, a single is sufficient as DC power supply.

[0087] Drawing 4 is the sectional view of the semiconductor chip 1 in which the part into which anode plate junction is performed was shown, and shows the sectional view at the time of cutting the center section of leadframe 4a of width-of-face W3 shown in drawing 3 to a longitudinal direction. In drawing 4, 2 shows the electrode of the rectangular parallelepiped of height h by width of face W2 of one side. Opening of the square whose one side is W2n is formed in the perimeter of this electrode 2, this opening avoids, and it adheres to insulating coat 2a on the semiconductor chip 1. Therefore, the gap of W2 n-W2 arises between an electrode 2 and insulating coat 2a.

[0088] The vertical dimension of the electrode 2 before are pressed by inner lead 4a and the part of the alternate long and short dash line shown with a dimension h is not deformed in the case of anode plate junction was expressed, and the upper part has projected only deltah from the insulating coat 2a page. Therefore, the semiconductor chip front face will adhere to insulating coat 2a by the thickness of (h-deltah).

[0089] Moreover, when anode plate junction is completed and an electrode 2 is pressed, an electrode 2 becomes as [height / which is shown as the continuous line of this drawing 4] (h-deltah). Although it will be crushed if an electrode 2 is pressed, and width of face naturally increases to a longitudinal direction, since the allowances of W2 n-W2 are between an electrode 2 and insulating coat 2a, the effect of the increment does not reach to an insulator layer 2.

[0090] However, when the compressive strain which press an electrode 2 and actually become deltah/h are produced, since it is the order of abbreviation 0.3, when a design stage examines and increment deltaW can be disregarded, it is good [increment deltaW of the width of face W2 of an electrode 2 is deltaW=nux (deltah/h), and / Poisson's ratio nu of an electrode 2] at this time also as W2 n=W2.

[0091] The part by which anode plate junction of inner lead 4a and the insulating coat 2a is carried out is actually the range of the anode plate junction fields l1 and l2 whose width-of-face W2n openings were pinched. Next, the reaction force produced in the anode plate junction force and electrode 2 which are produced in the anode plate junction fields l1 and l2 is explained to a detail with reference to drawing 5.

[0092] Drawing 5 explains the relation between the anode plate junction force Ffab produced to insulating coat 2a, and the reaction force Fel produced from an electrode 2, the magnitude of the anode plate junction force Ffab designs the magnitude of an electrode 2 so that it may be set to Ffab>>Fel compared with the reaction force Fel produced as reaction by electrode compression, and it is made to always be applied [drawing 5] to reaction force Fel by static simple compression.

[0093] Moreover, although the anode plate junction fields l1 and l2 are not drawn so that reaction force Fel may come to the core of the anode plate junction force Ffab of TOORU by drawing 5 since they are

not equal, it is desirable for Fel to come to the core of Ffab and to make it an electrode 2 come to the core of the anode plate joint of inner lead 4a ideally. However, as long as it is the design matter which may require the moment and compression for an electrode 2, Fel may be prepared outside the core of Ffab.

[0094] When anode plate junction is carried out, the reaction force Fel produced in an electrode 2 is expressed with Fel=Ex(deltah/h) xW2xW2 proportional to deltah/h. Here, E shows the elastic modulus (Young's modulus) decided by the ingredient physical properties which constitute an electrode 2.

[0095] The anode plate junction force Ffab is as a result of [of the **** breaking strength of the plane of composition when joining the boro-silicated glass and silicon which are insulating coat 2a] an observation, and is joined so firmly that fracture of a glass base material is shown. Therefore, since it is considered anode plate bonding strength sigmafab>=4kgf/mm2, it is set to junction force Ffab={W3x(l1+W2 n+l2)-W2 nxW2n} xsigmafab by anode plate junction. Now, considering Ffab/Fel, this value must become larger than 1 about the ratio of the anode plate junction force and reaction force. Here, Ffab/Fel is expressed with the following formulas.

[0096]

[Equation 1]

$$F_{tab}/F_{el}=\frac{\sigma_{tab}\times\{W3\times(l_1+W2n+l_2)-W2n\times W2n\}}{E\times(\Delta h/h)\times W2\times W2}$$

[0097] Ffab/Fel is expressed with the following formulas, when aluminum is adopted as the quality of the material of an electrode 2 and 2 is substituted E= 6300 kgf/mm.

[0098]

[Equation 2]

$$F_{tab}/F_{el}=\frac{4\times\{W3\times(l_1+W2n+l_2)-W2n\times W2n\}}{6300\times(\Delta h/h)\times W2\times W2}$$

[0099] If it is made to carry out the variation rate of it within a plastic domain when an electrode 2 receives compressive force since the breaking strength of an electrode 2 is 2 7 kgf(s)/mm, 1.1x10 to three or less will be the value which can be taken as deltah/h. Therefore, Ffab/Fel is expressed with the following formulas, when breaking strength is set up with twice as many allowances as this and the dimension of each part is decided as deltah/h=5x10-4.

[0100]

[Equation 3]

$$F_{tab}/F_{el}=1.27\frac{\{W3\times(l_1+W2n+l_2)-W2n\times W2n\}}{W2\times W2}$$

[0101] Here, since it is W3>=W2 n>=W2, if W3**W2 n**W2, the minimum Ffab/Fel will be obtained from the following formulas.

[0102]

[Equation 4]

$$F_{tab}/F_{el}=1.27\times(\frac{l_1+W2n+l_2}{W2}-1)>1$$

[0103] therefore, it is shown in drawing 4 that what is necessary is just to satisfy the conditions of an upper type — as (l1+W2 n+l2) — it is possible to make it larger than W2.

[0104] When deltah/h is set to 5x10-4 from the relation of W3, l1+l2+W2n, and /(W2 n-W2) W2 >= nuxdelta h/h that determines W2 in the case of an aluminum electrode so that it may be satisfied with this example of the above conditions, it is set to W2n>1.000165W2=W2+1.65x10-4xW2 from nu= 0.33. therefore, W — when making 2n larger than W2, a W2n dimension will be W1.65x10 to 4 times 2, and should just form opening in magnitude minuter than the dimension of an electrode 2.

[0105] If deltah/h=5x10-4 are adopted, it is necessary to set thickness of insulating coat 2a to h-delta

h=0.9995 and h. If thickness of insulating coat 2a is generally set to 25 micrometers, what carried out 125A piling to the thickness of insulating coat 2a will be made that what is necessary is just to design the height of an electrode to h= 25.0125 micrometers.

[0106] Since the dimension was decided so that deltah/h might be designed in the plastic deformation field of the component of an electrode 2 and it might be set to deltah/h=5x10−4, and the difference of the height of an insulating coat and an electrode became small with 25x5x10−4=125x10−4micrometer, the above needs to make the height of an electrode 2 with a precision sufficient on manufacture.

[0107] Since the precision on manufacture can be dropped and electrode height can be adjusted when using an electrode 2 across a plastic deformation field, it is good to make it the trapezoidal shape shown as the contact surface of an electrode 2 is made spherical as shown in (a) of drawing 6 , or shown in (b) of drawing 6 . or although mentioned later, it is shown in drawing 7 and drawing 8 — as — elasticity spherical to an electrode surface — a conductor (Hitoshi Handa) — laying — this elasticity — it is very good in the electrical installation of an inner lead and an electrode through a conductor.

[0108] In addition, in order to make the Ffab/Fel value by the bottom type larger than 1 here based on drawing 8 , a top view is shown in the semiconductor chip 1 at the time of making it W3>W2.

[0109]

[Equation 5]

$$\mathrm{Ftab}/\mathrm{Fel}=\frac{1.27\times\{W3\times(l_1+W2n+l_2)-W2n\times W2n\}}{W2\times W2}$$

[0110] And in order to enlarge the value of Ffab/Fel, it is effective to make W2 as small as possible and to enlarge W3 as much as possible. An A−A sectional view [in / in drawing 9 / drawing 8] and drawing 10 show the I−I cross section in drawing 8 . Although the condition that the core of the lengthwise direction of inner lead 4a and the junction core of an electrode 2 established in the front face of a semiconductor chip 1 were in agreement at the process in which drawing 8 − drawing 10 carry out anode plate junction is shown, it is necessary to take into consideration gap of center line I−I shown in drawing 8 , and gap of center line A−A at an assembly process.

[0111] Even if it produces these assembly errors, it considers that an electrode 2 does not deviate from the range where anode plate junction of the inner lead 4a is carried out, and the dimension of each part is decided. In drawing 8 − drawing 10 , Ffab and Fel are calculated as l2=400micrometer which is [dimension / of an electrode 2 / of one side / dimension / W2=50micrometer and / of opening / of one side] W3=300micrometer and each anode plate junction field in the thickness of W2n=51micrometer and insulating coat 2a about the width of face of h= 25 micrometers of h−delta, and inner lead 2a, and l1=400micrometer.

[0112] Consequently, it has the anode plate junction force of Ffab=1.01kgf, and is set to reaction force Fel=7.88gf by electrode compression. At this time, the planar pressure of the contact surface of an electrode 2 can be said to be sufficient planar pressure, in order to obtain an electric flow by 2 3.15 kgf(s)/mm. And it is set to Ffab/Fel=128.2 and sufficient junction force can be acquired. In addition, although the anode plate joint die length l1 and l2 made it differ and the electrode 2 explained one thing by drawing 10 , a good thing cannot be overemphasized even if two or more.

[0113] Drawing 11 shows the top view which looked at the condition of having joined the semiconductor chip 1 to inner lead 4a by the anode plate junction approach, from the top face of a semiconductor chip 1. The tip of inner lead 4a is extended over an electrode 2 in the front face of a semiconductor chip 1 so that clearly from this drawing. And anode plate junction is performed in the part which smeared away the tip of inner lead 4a. If drawing 49 which shows signs that the INA lead 4 and semiconductor chip 1 using the conventional wire bond conjugation method were joined, and the anode plate junction approach by this example are explained by comparison, and the anode plate junction approach is used, a gold streak 5, a die pad 41, and hanging and becoming unnecessary [lead 42] can understand easily.

[0114] Drawing 12 shows insulating coat 2a which formed opening in the parts of the electrode 2 arranged on the front face of a semiconductor chip 1, and an electrode 2. All the front faces of the

semiconductor chip 1 to which what it should be careful of here adhered insulating coat 2a are anode plate joinable fields, and it is the description that the anode plate joinable field where anode plate junction of the inner lead 4a is not carried out can also be freely used for the purpose.

[0115] Although the example 2. above and an example 1 showed the shape of a ball, and trapezoidal shape for the configuration of the contact surface of an electrode 2, effectiveness is the same if the conditions stated in the text irrespective of the configuration are filled also with the deformation electrode using a pyramid form and the side etch when etching and forming. When anode plate junction completes this, the area with which an electric flow is presented between inner lead 4a and electrode 2a should just be necessary minimum. What is necessary is to be able to perform only an electric flow, although the contact part of electrode 2a crushed by junction deforms as a broken line shows across a plastic zone as shown in (b) of drawing 6 in this case.

[0116] And if the physical properties of an electrode 2 are chosen accurately, even if an electrode 2 causes the plastic deformation by compression, the electric flow between an electrode 2 and inner lead 4a is normally maintainable. Even when it is the worst, a gold streak 5 is fused, and junction more stable than the method by wirebonding which makes this fused gold streak 5 recombine with the aluminum which is an electrode is acquired. The reason is because sufficiently firm mechanical junction is performed by anode plate junction in parts other than polar-zone 5 in inner lead 4a.

[0117] although it made into trapezoidal shape whether to make the contact surface of an electrode 2 spherical in the example 3. above-mentioned example 1, in order to secure greatly many amount of crush dimensions deltah between insulating coat 2a and an electrode 2, as shown in (a) of drawing 7 , it is effective in an electrode 2 to prepare corpuscle 2A of conductivity for example, such as gold and solder, which has a low elastic modulus, and it appears in it. When anode plate junction of the 2B is carried out in this drawing, the condition that corpuscle 2A would be crushed by the inner lead which is not illustrated, the electrode 2 would be joined to the inner lead, and it would be in switch-on by it is shown.

[0118] In (a) of drawing 7 , although the electrode 2 was made to project from a silicon substrate in opening of insulating coat 2a, it is shown that (b) of drawing 7 exposes an electrode 2 to a silicon substrate surface in opening, and only (h-deltah) is in a low location from the front face of insulating coat 2a about an electrode 2. Consequently, spherule 2C of the big path by thickness of electrode 2a can be inserted from conductive corpuscle 2A shown in (a) of drawing 7 . if configuration 2D after being crushed at this time assumes in a radius R that it is the cylinder of height (h-deltah) -- a conductor -- the relation with Ball sigma is expressed with the following formulas.

[0119]

[Equation 6]

$$R=\sqrt{\frac{4\,r^{3}}{3\times(h-\Delta h)}}$$

[0120] Here, if the radius r of a ball is made the same as the thickness (h-deltah) of insulating coat 2a, the path of configuration 2D which was able to be extended will be set to R=1.155r. That is, 15.5%R becomes large [before the radius r of inserted corpuscle 2C is crushed]. From this, the thickness (h-deltah) of insulating coat 2a can be manufactured, although manufacture precision is raised and it drops off.

[0121] Moreover, in order that this may just form more greatly than Path R dimension W2n of electrode opening of insulating coat 2a at the maximum, With the radius r of ball 2C, and the thickness (h-deltah) of insulating coat 2a For the path R of configuration 2D, it is pi(4/3) r3= (h-deltah) and pi-R 2 which changes. ... (A) Both sides are differentiated and they are 4pir2anddeltar=2pi(h-deltah) R-deltaR+pi-R2anddelta (h-deltah)... If the ratio of the (B) and (B) type and the (A) type is taken, it will become like the following formulas.

[0122]

[Equation 7]

$$\frac{1}{3}\cdot\frac{\Delta r}{r}=2\cdot\frac{\Delta R}{R}+\frac{\Delta(h-\Delta h)}{(h-\Delta h)} \quad \cdots (C)$$

$$(C) より \quad \frac{\Delta R}{R}=\frac{1}{2}\times\{\frac{1}{3}\cdot\frac{\Delta r}{r}-\frac{\Delta(h-\Delta h)}{(h-\Delta h)}\} \quad \cdots (D)$$

[0123] From the (D) type which developed the (C) type of several 7, the rate of change of the radius of the field which should be carried out electric junction is expressed with the right-hand side of the (D) type. That is, since deltar/r=**10%, delta(h-deltah)/(h-deltah) =**10%, then deltaR/R change only 6.7%, it is clear for accurate electrical installation to be possible. That is, the manufacture precision of corpuscle 2C and the manufacture precision of insulating coat 2a mean that the error of the radius of the part with which the electric junction after being crushed also as addressing ****** 10% is presented is as small as 6.7%.
[0124] (A) By the formula, since it was pir3=VBall (4/3), when it is set to VBall/pi x(h-deltah) =R2 and size is in the volume of a ball, and when there is an error also in an insulating coating thickness dimension (h-deltah), deltaR/R is expressed with the following formulas.
[0125]
[Equation 8]

$$\frac{\Delta R}{R}=\frac{1}{2\pi}\{\frac{\Delta V_{Ball}}{V_{Ball}}-\frac{\Delta(h-\Delta h)}{(h-\Delta h)}\}$$

[0126] Therefore, as long as VBall is conductive inclusion which has the volume which is not spherical, either, a bump is sufficient as it, what carried out the laminating of the electrode is sufficient as it, and it may make the quality of conductivity project towards an electrode 2 from a leadframe. The same effectiveness will be obtained if the conductive matter set to VBall in short is made to intervene between an electrode 2 and inner lead 4a. In drawing 6 and drawing 7 , although how to constitute an electrode 2 from an ideal dimension was described, if anode plate junction is actually performed, and the reaction force Fel of an electrode 2 cannot crush an electrode 2 by inner lead 4a greatly for delta h minutes, an unsealed part will be produced into the part which carries out anode plate junction.
[0127] However, if it kicks, even if an unsealed part is in about one electrode, when the mechanical bond strength of inner lead 4a and a semiconductor chip 1 is securable enough in the joined part with an area large enough which carries out anode plate junction, it is enough even if it sets up ** by the usual approach regardless of the precision of deltah.
[0128] About example 4. and the conductive matter inclusion of the polar zone, although the spherical corpuscles 2A and 2C of drawing 7 perfect in (a) and (b) explained, if the conditions stated in the above-mentioned example 3 are fulfilled, even if it is irregular configuration objects, such as a rectangular parallelepiped and a cube, the same effectiveness will be produced. The high thing of plasticity, liquefied conductive material like mercury, and conductive resin of aluminum, solder, gold, etc. are sufficient also about a physical-properties value.
[0129] However, it is higher than the modulus of elasticity of these quality of the materials in the quality of the materials of a semiconductor chip being silicon and GaAs, and since a semiconductor chip will fracture if conductive matter inclusion is formed, that which forms conductive matter inclusion with the quality of the material of a modulus of elasticity smaller than the modulus of elasticity E of the quality of the material of a semiconductor chip and which is boiled is desirable. Moreover, conductive resin etc. is sufficient as long as it is except a metal. However, that into which the diameter when crushing flows exceeding opening dimension W2n of insulating coat 2a is not desirable.
[0130] a part of semiconductor chip 1 front face explaining the pitch between the adjoining electrodes 2 it was decided in the magnitude of an electrode 2 that would be the former being made more to a ** pitch, and the miniaturization of a chip of it being attained, if drawing 13 uses the junction approach by this example — it is an enlarged drawing. A dimension in the case of using the dimension a between the

wiring conductors 21 in this drawing and the conventional conjugation method is contrasted, and drawing 51 is explained.

[0131] The pitch A between electrodes 2 is decided by drawing 51 with the dimension D of an electrode 2, and the dimension E of opening. However, if inner lead 4a and a semiconductor chip 1 are combined by the anode coupling approach by this example, each dimensions B and D of the electrode 2 shown in drawing 13 and each dimensions C and E of opening will be made small. This does not become being able to make very small A dimension between each inner lead 4a outside. Thus, it is because that dimensions B and D can be made small does not need to secure a large area that there should just be area which can take inner lead 4a and minimum electric junction as an electrode 2 in order to raise mechanical bond strength with inner lead 4a.

[0132] In addition, the relation between the area of an electrode 2 and the anode plate plane-of-composition product of all in NARIDO 4a is explained here with reference to drawing 13 , drawing 8 mentioned above, and drawing 12 . In drawing 12 , if the area of insulating coat 2a by which anode plate junction is carried out in the front face of a semiconductor chip 1 is expressed using the dimensions l1 and l2 shown in drawing 8 , W3, W2n, and W2, it will serve as {W3x(l1+W2 n+l2)-W2 nxW2n}. And since there are 19 anode plate junction fields in all in the number 19 of an electrode 2, the whole surface product of insulating coat 2a by which anode plate junction is carried out becomes 19x {W3x(l1+W2 n+l2)-W2 nxW2n}.

[0133] And since each area of an electrode 2 is 19xW2 nxW2n, if area of an electrode 2 is made small, the area of an anode plate junction field will become large, and the mechanical junction force Ffab will become large. Since W2n which determines the area of an electrode 2 is equivalent to D dimension shown in drawing 13 , if D dimension becomes small, it means that A dimension can be made small. Therefore, it is the most important element for attaining the purpose which enlarges the mechanical junction force Ffab to make W2n or D dimension small while contraction-izing a semiconductor chip.

[0134] With the anode plate conjugation method of this example, (a) of example 5. drawing 14 is what showed the example which constituted the semiconductor device without using mold resin, and shows a mall dress QFP package. It is what showed that the semi-conductor was constituted without (b) of drawing 14 using mold resin using anode plate junction of this invention similarly, and a mall dress QFP package is shown. Here, the alternate long and short dash line shown in each drawing is [0135] which shows the range of the mold which will be given if required in order to protect a semiconductor chip 1 from an external environment. the semiconductor device manufactured by the conventional wirebonding method since inner lead 4a was able to be directly joined to the front face of a semiconductor chip 1, it was able to fix, a part for the point of inner lead 4a was able to be pressed to an electrode and electric junction was taken by manufacturing a semiconductor device using an anode plate conjugation method -- like -- a gold streak -- the mold resin for fixing protection and the inner lead 4 of five part becomes unnecessary Moreover, since the external lead 44 can be bent from the edge part of a semiconductor chip 1 to a direct lower part, only the part of the mold resin which became unnecessary can miniaturize the configuration of a semiconductor device.

[0136] Similarly (a) of drawing 15 is the mall dress SOP (Small Outline Packge). TYPE I is shown. SOP TYPE II is omitting illustration. Although (a) of drawing 15 shows the thing in which a semiconductor chip 1 is mounted by face up and which made the external lead 44 the gull wing configuration like, it may bend up and a gull wing configuration may be formed, as a dotted line shows, so that a semiconductor chip 1 can mount by face down.

[0137] Similarly (b) of drawing 15 is a mall dress. J bend lead 44 is shown and signs that the external lead 44 can be caudad bent along with the edge of a semiconductor chip 1 are shown. It is also possible J bend external lead 44 shown in this drawing 15 as well as a gal UIGU configuration and to make with a reverse bend J lead.

[0138] (a) of drawing 16 shows what carries out face-up mounting of the QFP package which formed the gull wing external lead 44 in the mall dress. Although the drawing is omitted, SIL and DIP can apply it

to all the conventional packages. (b) of drawing 16 shows the condition of having carried out mold to the tip location of the external lead 44 shown in (a) of drawing 16 with mold resin 8. It is effective in the precision of the display flatness of the external lead 44 becoming good by sheathing by this mold resin 8.

[0139] Drawing 17 shows an example which applied the anode plate conjugation method by this example to the semiconductor device. As compared with drawing 43 which shows the semiconductor device made with the conventional conjugation method, it turns out by drawing 17 that a gold streak 5, a die pad 41, and the die bond material 6 are unnecessary. Moreover, it is also possible to carry out sheathing by mold resin 8 to the location which shows a semiconductor device with an alternate long and short dash line.

[0140] Drawing 18 shows the case where the anode plate conjugation method of this invention is used to a LOC (Lead On Chip) type. Drawing 19 shows the sectional view which carried out the cross section by the Wu U line of drawing 18 so that an anode plate joint might be known. 41' shows a heat sink. Since inner lead 4a is directly joined to an electrode 2 unlike connecting an inner lead 4 with an electrode 2 through a gold streak 5 so that it may understand in contrast with (a) of drawing 54 which shows the conventional LOC type, and (b), a semiconductor device reliable LOC type can be obtained. It is also possible to carry out sheathing of the semiconductor device by mold resin 8 to the location shown with the alternate long and short dash line of drawing 19.

[0141] Moreover, by using an anode plate conjugation method for drawing 20 and drawing 21 shows the example which can omit a die pad 41 and can obtain a LOC package. This is fixing the inner lead directly joined to the semiconductor chip 1 with mold resin 8, and can reduce a labor in the die pad 41 which supports a semiconductor chip 1.

[0142] An example which used anode plate junction is shown in a TCP package at drawing 22 . It is shown that a lead and junction of a chip can strengthen the conventional TCP package as compared with (a) of drawing 55 and (b). Drawing 23 shows the drawing to which the joint was expanded in more detail. Drawing 24 shows an example which used anode plate junction for high power IC. Drawing 25 shows the drawing to which the joint was expanded more. In this drawing, 41' shows a heat sink.

[0143] Although the leadframe 4 was made into the anode plate, the semiconductor chip 1 was used as cathode and anode plate junction was performed in the example 6. above and each example, the case where use a leadframe 4 as cathode, make a semiconductor chip into an anode plate, and anode plate junction is performed is explained. First, when making a semiconductor chip 1 into an anode plate, through hole 2T which reach the passivation insulator layer to which it adhered on the semiconductor chip 1 as shown in drawing 26 at a silicon substrate are prepared in the edge which avoided the electrode 2 on a semiconductor chip 1.

[0144] After preparing through hole 2T, it adheres on passivation insulator layer 2i in 2m of metallic films. Consequently, 2m of metallic films accumulates on through hole 2T, and a silicon substrate and 2m of metallic films flow. Thus, if it adheres to 2m of metallic films, the dimension of one side will prepare opening of the square of H1 in the perimeter of the location where an electrode 2 exists to 2m of metallic films, and passivation insulator layer 2i will be exposed.

[0145] Next, in this opening, the dimension of one side prepares in the perimeter of the location where an electrode 2 similarly exists to passivation insulator layer 2i to which opening of the square of H2 was exposed, and an electrode 2 is exposed. Here, the dimension H2 of opening is determined according to the dimension of one side of the electrode height of the square formed in the point of inner lead 4a mentioned later. A dimension H1 is determined corresponding to push crushing width of face when an electrode height is pressed by the electrode 2 and deforms plastically.

[0146] Next, the formation approach of the leadframe when performing anode plate junction by using a leadframe 4 as cathode is explained with reference to drawing 27 . In this drawing, electrode height 2P of the square of P (P<H2) are prepared for width of face of one side in all in the anode plate junction field at the tip of inner lead 4a in the location of the electrode 2 on a semiconductor chip 1. Furthermore, electrode height 2P are avoided in an anode plate junction field, and it adheres to insulating coat 2a.

[0147] Drawing 28 is the sectional view showing a condition when the semiconductor chip 1 shown in drawing 26 is made into an anode plate and anode plate junction is completed by using as cathode inner lead 4a shown in drawing 27 . In this drawing, the sum total dimension of the thickness of insulating coat 2a prepared in inner lead 4a, the thickness of passivation insulator layer 2i prepared in the front face of a semiconductor chip 1, and the thickness of 2m of metal membranes With constituting so that only deltah may become small from the sum total dimension of the thickness of the electrode 2 prepared in the thickness dimension and semiconductor chip 1 of electrode height 2P which were prepared in the leadframe 4 When anode plate junction of the inner lead 4a is carried out at a semiconductor chip 1, to an electrode 2, only deltah is compressed and electrode height 2P are joined.
[0148] Although the example 7. above and an example 6 were made to carry out the pressure welding of the electrode height 2P prepared in the anode plate junction field of inner lead 4a to the electrode 2 exposed to the opening base on a semiconductor chip 1, an electrode 2 may be made to project and the anode plate junction field of inner lead 4a may be made to carry out the pressure welding of this electrode 2 made to project.
[0149] Drawing 29 is the sectional view of the semiconductor chip 1 in which the dimension of one side makes the top face of the electrode 2 of the square of P project from the maximum top face of 2m of metallic films made to adhere to passivation insulator layer 2i of a semiconductor chip 1, and the configuration in which the dimension of one side prepared opening of H1 centering on the electrode 2 at passivation insulator layer 2i is shown. About other configurations, it is the same as that of drawing 26 .
[0150] Drawing 30 is the perspective view showing the configuration of inner lead 4a, and it has prepared opening which consists of a crevice of the opening dimension H2 in the location which should join to an electrode 2 on insulating coat 2a, and should take a flow while it will adhere insulating coat 2a by which it is electrified slightly, if it is heated in the anode plate junction field of this inner lead 4a. The front face of a leadframe 4 exists in the bottom of opening.
[0151] Drawing 31 is the sectional view in which making into an anode plate the semiconductor chip 1 shown in drawing 29 , and showing the condition when carrying out the completion of anode plate junction by using as cathode inner lead 4a shown in drawing 30 . In this drawing, insulating coat 2a, passivation insulator layer 2i, and the sum total dimension of the thickness of 2m of metallic films are constituting so that only deltah's may become small from the sum total dimension of the thickness of an electrode 2, when anode plate junction of the inner lead 4a is carried out at a semiconductor chip 1, in an electrode 2, the compression set only of the deltah is carried out and electric junction of electrode height 2P and the electrode 2 is carried out.
[0152] Although electric junction was carried out in the example 8. above and the example 7 by carrying out anode plate junction of inner lead 4a and the semiconductor chip 1, and carrying out the pressure welding of inner lead 4a and the electrode on a semiconductor chip 1, a semiconductor chip 1 may be mounted in a wiring insulating substrate by carrying out anode plate junction of the semiconductor chip 1 at two or more coincidence at a wiring insulating substrate.
[0153] Drawing 32 is a perspective view which explains how to carry out anode plate junction of the semiconductor chip to a wiring insulating substrate. In drawing, 3A-3C are the electrodes by which isolation arrangement was carried out on the semiconductor chip 1. Only deltah has projected the front face of these electrodes 3A-3C from the front face of insulating coat 2a to which the chip front face adhered.
[0154] the conductor by which 70 is a wiring insulating substrate and a pressure welding is carried out to the electrodes 3A-3C prepared on this wiring insulating substrate 70 at the semiconductor chip 1 — the conductor by which anode plate junction is carried out with insulating coat 2a in addition to wiring 3AA-3cc — the piece of anode plate junction of wiring and this ingredient (copper foil plate) — patterning of the conductors 4A and 4B is carried out.
[0155] the electrodes 3A, 3B, and 3C of the semiconductor chip 1 constituted as mentioned above — the conductor of the wiring insulating substrate 70 — alignment is adjusted so that it may be in

agreement with wiring 3AA, 3BB, and three cc. at this time, it is shown in drawing 33 — as — Electrodes 3A–3C — a conductor — wiring 3AA–3cc is countered — as — a location — setting up — anode plate junction — a conductor — Pieces 4A and 4B set up a location so that insulator layer 2a prepared on the front face of a semiconductor chip 1 may be countered.

[0156] the cathode of the direct current voltage supply which lay a semiconductor chip 1 on top of the wiring insulating substrate 70, and are not illustrated to a semiconductor chip 1 after alignment is completed — connecting — the piece of anode plate junction — the condition connected the anode plate of direct current voltage supply to Conductors 4A and 4B — anode plate junction — a conductor — when piece 4A is heated, it is shown in drawing 34 — as — anode plate junction — anode plate junction — a conductor — it is carried out between Pieces 4A and 4B and insulating coat 2a prepared on the semiconductor chip 1.

[0157] consequently, a conductor — wiring 3AA–3cc, compression of deltah is received from polar zone 3A–3C, and electric junction is made. furthermore, a semiconductor chip 1 and the wiring insulating substrate 70 — insulating coat 2a and anode plate junction — a conductor — it is firmly joined among Pieces 4A and 4B.

[0158] example 9. drawing 32 and drawing 33 — the wiring insulating–substrate 70 side — the piece of anode plate junction, although anode plate junction was performed in the condition of having formed Conductors 4A and 4B, having prepared insulating coat 2a in the semiconductor chip front face, and having considered as the anode plate conversely, in order to make a semiconductor chip side into an anode plate by using wiring insulating–substrate side 70 as cathode, drawing 29 shows — as — as sufficient insulation for the electric insulation film around an electrode 2 as an electrode 2 — taking — anode plate junction — a conductor — a piece (metallic film) is adhered. and — the wiring insulating substrate 70 — wiring — a conductor — 3AA–3cc is avoided and insulating coat 2a is adhered.

[0159] The anode plate of the direct current voltage supply which will pile up both sides and will not be illustrated to a semiconductor chip 1 if positioning with 3AA–3cc is performed is connected. then, the electrode 2 of a semiconductor chip 1 and wiring of the wiring insulating substrate 70 — a conductor — the piece of anode plate junction — Conductors 4A and 4B — cathode — connecting — insulating coat 2a and anode plate junction — a conductor — the anode plate junction between Pieces 4A and 4B — carrying out — electrode 2a and wiring — a conductor — electric junction of 3AA–3cc is performed.

Example 10

[0160] (c) of (a) – drawing 35 of drawing 35 is the top view and detail drawing showing the configuration of the leadframe in the case of manufacturing a semiconductor device by the anode plate junction approach by this example. (a) of drawing 35 shows the example which constituted the lead group in eight–piece continuation. And 3 shows a leadframe frame. (b) of drawing 35 is drawing which expanded the part of "A" in (a) of drawing 35 . In drawing, the inner lead which 3 omitted the leadframe frame and the tip where 4a is joined to a semiconductor chip, and was shown, and 44 show an outer lead. (c) of drawing 35 shows the inner lead group of the point of inner lead 4a omitted and shown by (b) of drawing 35

[0161] From that by which the tip of an inner lead was viewed although 4 showed the inner lead in (c) of drawing 35 , although you may extend to a core side, in order to show in contrast with drawing 42 which shows the conventional inner lead, simple is carried out and it is shown. In (a) of drawing 35 , a die pad 41 and a die pad are supported and hung, and lead 42 is not needed. Therefore, spacing of an inner lead can be expanded and can be made with allowances. Moreover, since there is no die pad 41, a center section can take about and carry out an inner lead freely.

[0162]

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] It is the sectional view of the semiconductor chip explaining the anode plate conjugation method by one example of this invention.
[Drawing 2] It is the sectional view of the semiconductor chip explaining the anode plate conjugation method by one example of this invention.
[Drawing 3] It is the top view of the semiconductor chip in which the condition of having joined the electrode of a semiconductor chip and the inner lead of a leadframe with the anode plate conjugation method by this example was shown.
[Drawing 4] It is the sectional view of the semiconductor chip in which the condition of having joined the electrode of a semiconductor chip and the inner lead of a leadframe with the anode plate conjugation method by this example was shown.
[Drawing 5] It is the sectional view of the semiconductor chip explaining distribution of the load applied to a semiconductor chip front face from an inner lead at the time of anode plate junction.
[Drawing 6] It is the sectional view of the semiconductor chip in which the configuration of the electrode formed on the semiconductor chip was shown.
[Drawing 7] It is the sectional view of the semiconductor chip in which the configuration of the inclusion of the conductive matter placed between in NARI and an electrode and the configuration after deformation were shown.
[Drawing 8] It is the top view of the semiconductor chip which explains the junction condition of an inner lead and an electrode in this example to a detail.
[Drawing 9] It is the sectional view showing the cutting plane in a part for the AA line part in drawing 8 .
[Drawing 10] It is the sectional view showing the cutting plane in a part for the II line part in drawing 8 .
[Drawing 11] It is the top view of the semiconductor chip in which the anode plate junction condition of the inner lead on the semiconductor chip in this example is shown.
[Drawing 12] It is the top view of the semiconductor chip in which arrangement of the electrode on the semiconductor chip in this example is shown.
[Drawing 13] In order to explain the detail of the electrode joint in drawing 11 , it is the top view which expanded some semiconductor chips.
[Drawing 14] It is the perspective view of a semiconductor device the QFP type which joined and manufactured the electrode and the inner lead with the anode plate conjugation method, and SOP type.
[Drawing 15] It is the perspective view of the semiconductor device of other types which joined and manufactured the electrode and the inner lead with the anode plate conjugation method.
[Drawing 16] It is the perspective view of the example of the complete-change form of a QFP type semiconductor device which joined and manufactured the electrode and the inner lead with the anode plate conjugation method.
[Drawing 17] It is the sectional view of the semiconductor device in which the joint of the electrode of a semiconductor device and inner lead which were manufactured with the anode plate conjugation method is expanded and shown.
[Drawing 18] It is the perspective view of the semiconductor device in which the internal structure of

the semiconductor device manufactured with the anode plate conjugation method is shown.
[Drawing 19] It is the sectional view of the semiconductor device in which the cutting plane for a UU line part of drawing 18 is shown.
[Drawing 20] It is the perspective view of the semiconductor device in which the internal structure of the semiconductor device which made the die pad unnecessary with the anode plate conjugation method is shown.
[Drawing 21] It is the sectional view of the semiconductor device in which the EE cutting plane in drawing 20 is shown.
[Drawing 22] It is the sectional view of the semiconductor device by the TAB technique manufactured using the anode plate conjugation method.
[Drawing 23] It is the sectional view of the semiconductor device in which the anode plate joint in drawing 22 was expanded and shown.
[Drawing 24] It is the sectional view of a high power semiconductor device which manufactured using the anode plate conjugation method.
[Drawing 25] It is the sectional view of the semiconductor device in which the anode plate joint in drawing 25 was expanded and shown.
[Drawing 26] It is the sectional view of the semiconductor chip in other examples.
[Drawing 27] It is the perspective view showing the tip configuration of the inner lead which carries out anode plate junction in the semiconductor chip in drawing 26 .
[Drawing 28] It is the sectional view of the semiconductor chip in which the condition of having carried out anode plate junction of the inner lead shown in the semiconductor chip shown in drawing 26 at drawing 27 is shown.
[Drawing 29] It is the sectional view of the semiconductor chip in other examples.
[Drawing 30] It is the perspective view showing the tip configuration of the inner lead which carries out anode plate junction in the semiconductor chip in drawing 29 .
[Drawing 31] It is the sectional view of the semiconductor chip in which the condition of having carried out anode plate junction of the inner lead shown in the semiconductor chip shown in drawing 29 at drawing 30 is shown.
[Drawing 32] It is the perspective view showing signs that a semiconductor chip is mounted with an anode plate conjugation method in a wiring substrate.
[Drawing 33] It is the sectional view of the wiring substrate and semiconductor chip explaining the alignment of the wiring substrate and semiconductor chip in drawing 32 .
[Drawing 34] It is the sectional view of the wiring substrate and semiconductor chip which show the condition of having mounted the semiconductor chip with the anode plate conjugation method to the wiring substrate in drawing 32 .
[Drawing 35] It is the top view in which the flat-surface configuration of the leadframe used in case a semiconductor device is manufactured with an anode plate conjugation method is shown.
[Drawing 36] They are the top view of the wiring substrate used in case a multilayer laminating wiring substrate is manufactured with an anode plate conjugation method, and the sectional view of the completed multilayer laminating wiring substrate.
[Drawing 37] an anode plate conjugation method — the lead for external connection — wiring — it is the perspective view explaining signs that it joins to a conductor of a semiconductor chip.
[Drawing 38] It is the perspective view and sectional view showing the outline of a semiconductor device in which the ball grid array was used for the lead for external connection.
[Drawing 39] It is the perspective view explaining the conventional wire BONJINGU approach of a semiconductor chip.
[Drawing 40] It is the sectional view of the semiconductor chip explaining wirebonding by the gold streak.
[Drawing 41] It is the top view which expanded the top view of a leadframe, and its part to the former.
[Drawing 42] It is the top view which expanded the part of the inner lead in the conventional leadframe.

[Drawing 43] It is the sectional view showing some semiconductor devices manufactured by wirebonding.
[Drawing 44] It is the sectional view which expanded the wirebonding part in drawing 43 .
[Drawing 45] the gold streak to an electrode — it is a sectional view explaining the junction condition of a ball.
[Drawing 46] a gold streak -- it is a sectional view explaining the bonding condition of a ball.
[Drawing 47] It is a sectional view explaining the stitch-bonding condition of a gold streak.
[Drawing 48] It is the sectional view of the semiconductor device explaining the process of wirebonding.
[Drawing 49] Top view ****** of the semiconductor chip in which the junction condition of an inner lead and an electrode by wirebonding is shown.
[Drawing 50] It is the top view of the semiconductor chip in which the arrangement condition of the electrode on a semiconductor chip is shown.
[Drawing 51] It is the top view of the semiconductor chip in which the arrangement and the dimension of an electrode on a semiconductor chip were shown.
[Drawing 52] They are an electrode, a gold streak, and the top view having shown the dimension between inner leads.
[Drawing 53] It is a side elevation for a golden line part in drawing 52 .
[Drawing 54] It is the perspective view and sectional view of a semiconductor device which manufactured using wirebonding.
[Drawing 55] It is the sectional view which expanded the sectional view and BONDEIGU part of a semiconductor device which were manufactured with the TAB technique.
[Drawing 56] It is drawing explaining the anode plate junction approach.
[Drawing 57] It is drawing explaining other anode plate junction approaches.
[Drawing 58] It is the top view of the wiring substrate used for the conventional multilayer laminated circuit board.
[Drawing 59] It is the sectional view of the conventional multilayer laminated circuit board.
[Description of Notations]
1 the piece of a semiconductor chip, 2 wiring insulating-substrate, 90, and 90A metal, and B bump. Electrode and 2a An insulating coat and two a1 An anode plate junction region, 2A, and 2B Corpuscle and 2m A metallic film and 2P The letter electrode of a projection, and 3A-3C An electrode and 3AA-3cc wiring — a conductor, and 4A and 4B Piece of anode plate junction, and 4a An inner lead and 70

[Translation done.]